FIG.1
PRIOR ART

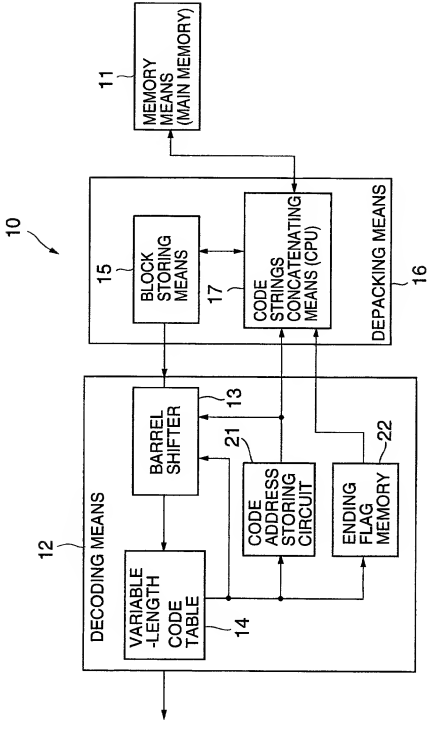


FIG.2

ITEMS	BUFFER MEMORY CAPACITY	ACCESS FREQUENCY OF MAIN MEMORY
GENERAL METHOD	(4400bit)	—
JPA.No 8-275162 (WITH BUFFER)	(3040bit)	LOW
JPA.No 8-275162 (WITHOUT BUFFER)	(~0bit)	HIGH
EMBODIMENT OF THIS INVENTION	(112bit)	LOW

FIG.3

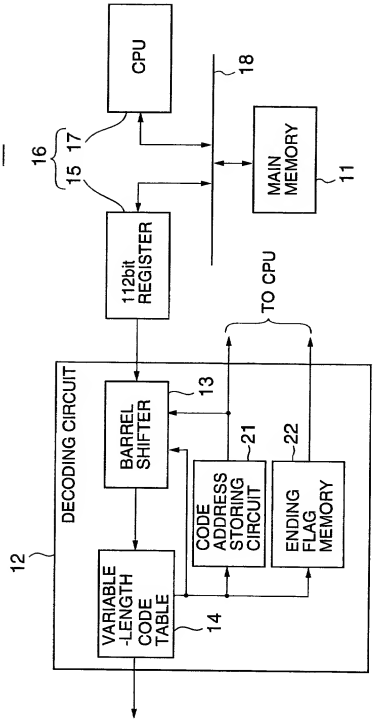


FIG.4

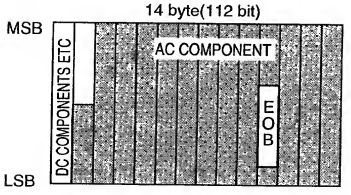


FIG.5

FIG.6A

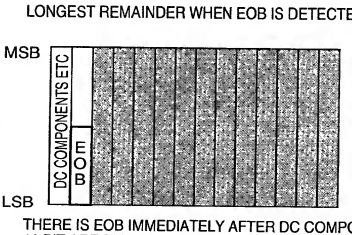


FIG.6B

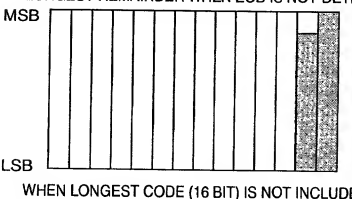


FIG.7A

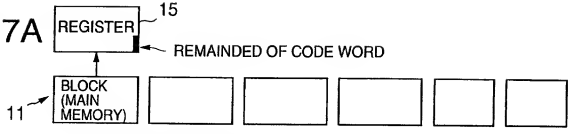


FIG.7B

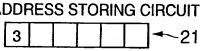


FIG.7C

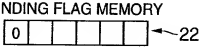


FIG.8A

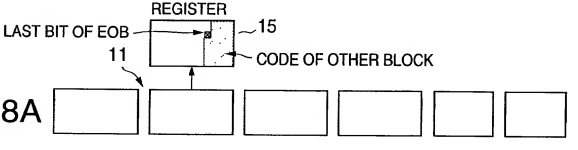


FIG.8B

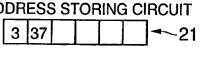


FIG.8C

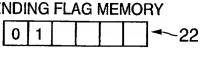


FIG.9A

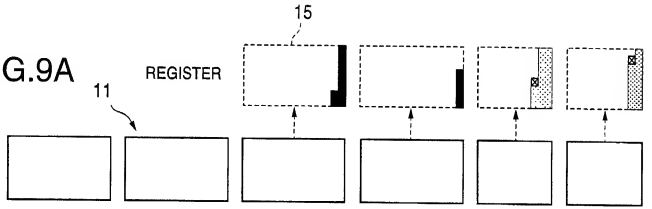


FIG.9B

ADDRESS STORING CIRCUIT

3	37	10	5	19	14

21

FIG.9C

ENDING FLAG MEMORY

0	1	0	0	1	1

22

FIG.10A

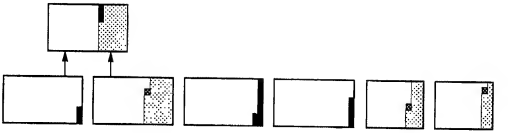


FIG.10B

ADDRESS STORING CIRCUIT

3	37	10	5	19	14

~ 21

FIG.10C

ENDING FLAG MEMORY

0	1	0	0	1	1

~ 22

FIG.11A

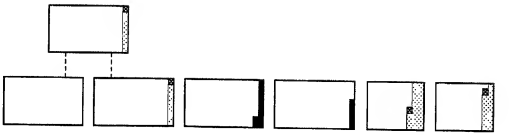


FIG.11B

ADDRESS STORING CIRCUIT

0	7	10	5	19	14

~ 21

FIG.11C

ENDING FLAG MEMORY

1	1	0	0	1	1

~ 22

FIG.12A

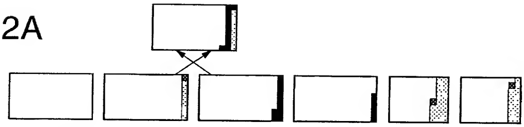


FIG.12B

ADDRESS STORING CIRCUIT

0	7	10	5	19	14

~21

FIG.12C

ENDING FLAG MEMORY

1	1	0	0	1	1

~22

FIG.13A

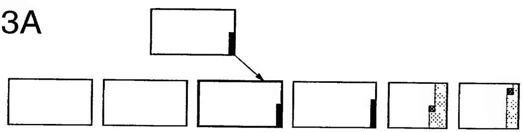


FIG.13B

ADDRESS STORING CIRCUIT

0	0	4	5	19	14

~21

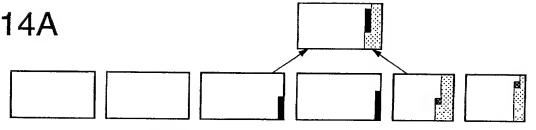
FIG.13C

ENDING FLAG MEMORY

1	1	0	0	1	1

~22

FIG.14A



ADDRESS STORING CIRCUIT

FIG.14B

0	0	4	5	19	14

~ 21

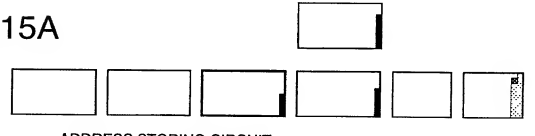
ENDING FLAG MEMORY

FIG.14C

1	1	0	0	1	1

~ 22

FIG.15A



ADDRESS STORING CIRCUIT

FIG.15B

0	0	6	5	0	14

~ 21

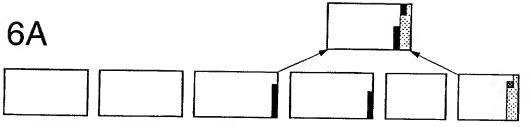
ENDING FLAG MEMORY

FIG.15C

1	1	0	0	1	1

~ 22

FIG.16A



ADDRESS STORING CIRCUIT

FIG.16B

0	0	6	5	0	14

~ 21

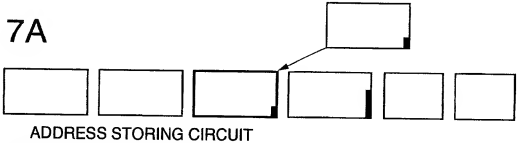
ENDING FLAG MEMORY

FIG.16C

1	1	0	0	1	1

~ 22

FIG.17A



ADDRESS STORING CIRCUIT

FIG.17B

0	0	2	5	0	0

~ 21

ENDING FLAG MEMORY

FIG.17C

1	1	0	0	1	1

~ 22

MEMORY ACCESS FREQUENCY IN PRIOR ART

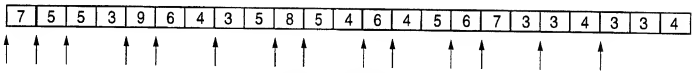


FIG.18A

MEMORY ACCESS FREQUENCY OF THIS INVENTION

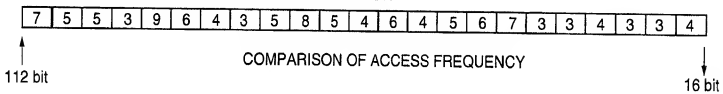


FIG.18B

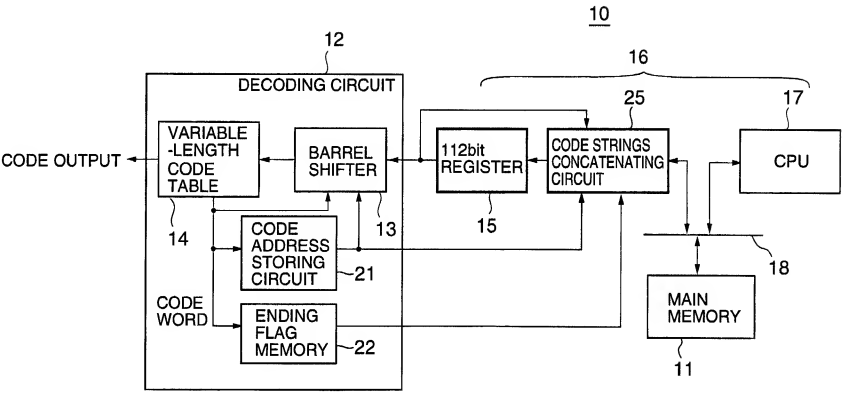


FIG.19

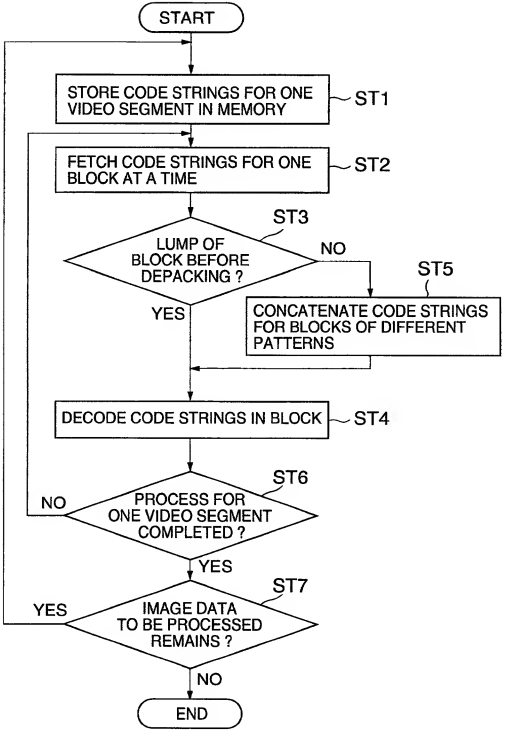


FIG.20

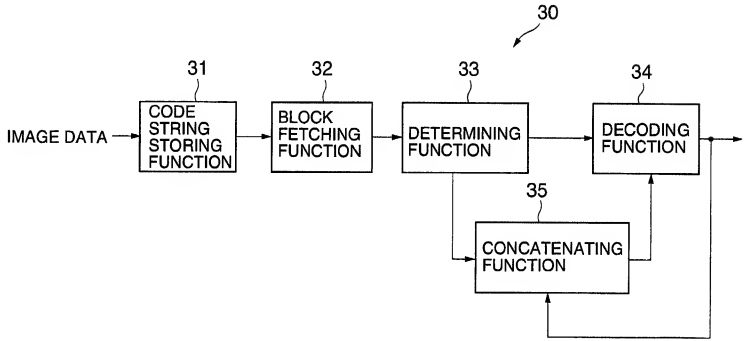


FIG.21